

## PROCESS FOR DESIGNING COMPARATORS AND ADDERS OF SMALL DEPTH

### ABSTRACT OF THE DISCLOSURE

Logic circuits for logical operations, based on  
5 a function  $f_N = x_1 \text{ OR } (x_2 \text{ AND } (x_3 \text{ OR } (x_4 \text{ AND } \dots x_N \dots)))$   
or  $f'_N = x_1 \text{ AND } (x_2 \text{ OR } (x_3 \text{ AND } (x_4 \text{ OR } \dots x_N \dots)))$ , are  
designed by defining a top portion of the logic  
circuit based on a pre-selected pattern of 2-input \$  
and @ gates. The top portion has N inputs and  
10 approximately  $N/3$  outputs. A smaller logic circuit is  
defined having approximately  $N/3$  inputs coupled to the  
outputs of the top portion. In one embodiment, the  
circuit is designed for a circuit having  $N'$  inputs,  
where  $N'$  is  $3^n$  or  $2*3^n$ , and the  $N'-N$  most significant  
15 inputs are set to fixed values. The extra gates are  
removed resulting in a minimum depth circuit. In  
another embodiment, the depth is further reduced in  
some cases by designing a circuit for  $N-1$  inputs and  
transforming the circuit to an  $N$ -input circuit. The \$  
20 and @ gates are converted to AND and/or OR gates,  
depending on the function.